ZIA KHAN

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DESIGN ENABLEMENT ENGINEER

Results-driven engineering leader with extensive expertise in design enablement, CAD tool development, and advanced CPU and GPU design methodologies. Proven track record of optimizing design flows, automating processes, and driving efficiency improvements. Adept at collaborating with cross-functional teams to enhance productivity and innovation in high-performance semiconductor designs. Management expertise in managing design and EDA teams in driving solutions, formulating operational plans, and delivering results.

CORE COMPETENCIES

CAD Tool Development & Automation | Scripting | Technology & Roadmaps | Leadership & Mentoring | EDA Vendor Collaboration | Problem Solving | CPU & ASIC Design Methodologies | Verilog | RTL Design | Physical Synthesis | Place and Route | Low Power | Timing Convergence | Verification | Formal Verification | Equivalence Checking| Power Optimization | Standard Cells | ASIC | SoC | Design Technology Co-optimization (DTCO) | Power-Performance-Area (PPA) Improvement | Machine Learning (ML) Enablement

PROFESSIONAL EXPERIENCE

Intel Corp, Folsom, CA Nov 2021 – Nov 2024

Principal Engineer, Design Enablement, Foundational IP, Production Libraries, 2023 – 2024

* Developed and optimized CAD tools and methodologies for next-generation (18A & 14A) libraries.
* Analyzed libraries for PPA improvements. Defined new cell families for high-performance applications that show 3% timing and 5+% area improvement.

Principal Engineer, Design Methodology, Xeon Engineering Group, 2021 – 2023

* Led the design flow and methodology for the next-generation Xeon processor design including physical implementation, formal verification, and regression testing.
* Spearheaded DTCO initiatives, optimizing standard cell usage to enhance library performance.
* Chaired EDA vendor collaboration meetings to drive strategic initiatives including ML-based solutions.

Synopsys Inc, Mountain View, CA May 2008 – July 2021

Technical Lead (Library Analysis) Program Management Group, 2012 – 2021

* Led Library Analysis team focusing on design technology co-optimization (DTCO) for improving standard cell libraries for PPA benefits, optimal synthesis, and P&R performance improvement.
* Provided consulting to several key internal and external customers to enhance their libraries.
* Developed new cell architectures for improving PPA.
* Directed Fusion Compiler enhancements to improve design quality.

Program Manager (Foundry), Program Management Group, 2010 – 2012

* Enabled a key foundry customer on 28- 20- and 16nm process technologies.
* Facilitated the introduction of new technologies such as double patterning and new routing features to support advanced process rules.

Senior Manager, Corporate Applications Engineering - Design Compiler, 2008 – 2010

* Managed global EDA support team across five international locations, delivering major software releases on schedule.
* Oversaw product planning, defined new capabilities, and managed customer relationships to meet the evolving needs of leading customers, provided technical content for conferences & trade shows, and did customer presentations.
* Supervised several successful customer engagements on leading-edge SoC designs using ARM processors focusing on performance, low power, and timing closure.

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Intel Corp, Folsom, CA 2005 – 2007

Application Engineering Manager, Design & Technology Solutions, 2006 - 2007

* Led back-end (synthesis, place & route, timing, and clocking) team that supported multiple CPU design teams using leading edge 45- and 32-nm processes. The team successfully enabled tapeouts of several leading CPU projects (Penryn, Nehalem, Westmere).
* Developed common design methodology for a variety of graphics and CPU designs using the best of in-house and external EDA solutions. This included defining development goals for internal and external teams, managing interfaces, and delivering to a committed schedule.

Technical Program Manager - Design & Technology Solutions, 2005 - 2005

* Analyzed 30+ vendors and developed a plan to use ESL for future processors and SoC designs. Subsequently, a new division was formed to create IPs for SoC designs.
* Worked on key EDA initiatives to streamline CAD tools across the company to enable reuse of design methodologies. Worked with several processor teams to ease the adoption of IC Compiler in CPU designs. This allowed Intel to do volume software purchases and save millions of CAD dollars.

ADDITIONAL PROFESSIONAL EXPERIENCE

Intel Corp, Folsom CA

Senior Staff Engineer, Folsom Design Center

Staff Engineer - Graphics Component Division

Staff Engineer, DA Manager - Platform & PCI Component Division

EDUCATION

Doctor of Philosophy (PhD), Electrical Engineering

Virginia Polytechnic Institute & State University, Blacksburg, VA

Master of Science (MS), Electrical Engineering

University of Kentucky, Lexington, KY

PATENTS & PUBLICATIONS

* 6 Patents in design methodologies, circuit optimization, and automated placement algorithms.
* 30+ technical papers at leading industry conferences.
* 3 invited keynote talks.

TECHNICAL LEADERSHIP & INNOVATION

* Mentor and technical advisor for junior engineers in design methodology and automation.
* Expert in integrating emerging technologies, including ML-based design solutions, to enhance CPU design workflows.